# Notice of References Cited

| Application/Control No. 09/590,584 | Applicant(s)/Patent Under Reexamination LY ET AL. | |
|---|---|---|
| Examiner A. M. Thompson | Art Unit 2825 | Page 1 of 5 |

## U.S. PATENT DOCUMENTS

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US-6,044,023 | 03-2000 | Proebsting | 365/189.01 |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

## FOREIGN PATENT DOCUMENTS

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
| | O | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

## NON-PATENT DOCUMENTS

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| * | U | Ly et al., Scheduling Using Behavioral Templates, Proceedings of the 32nd ACM/IEEE Conference on Design Automation, page 101-106, June 1995. |
| | V | Knapp et al., Behavioral Synthesis Methodology for HDL-Based Specification and Validation, Proceedings of the ACM/IEEE Conference on Design Automation, pages 286-291, June 1995. |
| | W | A. Stoll et al., Flexible Timing Specification in a VHDL Synthesis Subset, EURO-DAC Design Automation Conference, pages 610-615, September 1992. |
| | X | Y. Hu et al., Lower Bounds on the Iteration Time and the Number of Resources for Functional Pipelined Data Flow Graphs, IEEE International Conference on Computer Design: VLSI in Computers and Processors, pages 21-24, October 1993. |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| **Notice of References Cited** | 09/590,584 | LY ET AL. |
| | Examiner<br>A. M. Thompson | Art Unit<br>2825 | Page 2 of 5 |

## U.S. PATENT DOCUMENTS

| * | | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US- | | . | |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

## FOREIGN PATENT DOCUMENTS

| * | | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
| | O | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

## NON-PATENT DOCUMENTS

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | M. Koster et al., ASIC Design Using the High-Level Synthesis System CALLAS: A Case Study, 1990 IEEE International Conference on Computer Design: VLSI in Computers and Processors, pages 141-146, September 1990. |
| | V | R. Camposano et al., VHDL as Input for High-Level Synthesis, IEEE Design & Test of Computers, Volume 8, Issue 1, pag s 43 49, March 1991. |
| | W | F. Brewer et al., Chippe: A System for Constraint Driven Behavioral Synthesis, IEEE Computer-Aided Design of Integrated Circuits and Systems, Volume 9, Issue 7, pages 681-695, July 1990. |
| | X | D.A. Lobo et al., Generating Pipelined Datapaths Using Reduction Techniques to Shorten Critical Paths, 1992 EURO-DAC Design Automation Conference, pages 390-395, September 1992. |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

| | Notice of References Cited | Application/Control No. 09/590,584 | Applicant(s)/Patent Under Reexamination LY ET AL. | |
|---|---|---|---|---|
| | | Examiner A. M. Thompson | Art Unit 2825 | Page 3 of 5 |

## U.S. PATENT DOCUMENTS

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US- | | | |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | nn |
| | L | US- | | | |
| | M | US- | | | |

## FOREIGN PATENT DOCUMENTS

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
| | O | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

## NON-PATENT DOCUMENTS

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | C.-T. Hwang et al., A Formal Approach to the Scheduling Problem in High Level Synthesis, IEEE Transactions on Comput r-Aided Design of Integrated Circuits and Systems, Volume 10, Issue 4, April 1991. |
| | V | K. Kukcakar et al., CHOP: A Constraint-Driven System Level Partitioner, Proceedings of the 28th Conference on ACM/IEEE Design Automation, pages 514-519, June 1991. |
| | W | A. Stoll et al., High-Level Synthesis from VHDL with Exact Timing Constraints, Proceedings of the 29th ACM/IEEE Confer nc on Design Automation, pages 188-193, July 1992. |
| | X | C-T Hwang et al., Scheduling for Functional Pipelining and Loop Winding, Proceedings of the 28th Conference on ACM/IEE Design Automation Conference, pages 764-769, June 1991. |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

**U.S. PATENT DOCUMENTS**

| * | | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US- | | | |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
| | O | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | N. When et al., Scheduling of Behavioral VHDL by Retiming Techniques, Proceedings of the 1994 Conference on Europ an Design Automation, pages 546-551, September 1994. |
| | V | M. Valle et al., A VHDL-based Design Methodology: The Design Experience of a High Performance ASIC Chip, Proceedings o the 1994 Conference on Design Automation, pages 664-669, September 1994. |
| | W | R. Camposano et al., Synthesizing Circuits From Behavioral Descriptions, IEEE Transactions On Computer-Aided Design, pages 171-180, February 1989. |
| * | X | D. Gajski et al., High-Level Synthesis, Introduction to Chip and System Design, 1992, Kluwer Academic Publishers. |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

## Notice of References Cited

| Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|
| 09/590,584 | LY ET AL. |

| Examiner | Art Unit | |
|---|---|---|
| A. M. Thompson | 2825 | Page 5 of 5 |

### U.S. PATENT DOCUMENTS

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US- | | | |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

### FOREIGN PATENT DOCUMENTS

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
| | O | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

### NON-PATENT DOCUMENTS

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | W. Glunz et al., VHDL for High-Level Synthesis of Digital Systems, 1st European Conference on VHDL Models, pages 1-11, September 1990. |
| | V | S. Bakshi et al., Component Selection for High-Performance Pipelines, IEEE Transactions on Very Large Integration (VLSI) Systems, Vol. 4, No. 2, pages 181-194, June 1996. |
| | W | D. Wong et al., Designing High-Performance Digital Cirucits Using Wave Pipelining: Algorithms and Practical Experiences, IEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 12, No.1, pages 25-46, January 1993. |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.